SINGLE 2.2 V OPERATION MMIC POWER AMPLIFIER UTILIZING $SrTiO_3$ CAPACITORS FOR 2.4GHz WIRELESS COMMUNICATION SYSTEMS

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Abstract

This paper describes single 2.2 V operation of a two-stage MMIC power amplifier for 2.4GHz wireless local area network applications. The MMIC with 0.76 X 0.96 mm^2 area are composed of n-AlGaAs/ InGaAs/n-AlGaAs FETs with a shallow threshold voltage of -0.24 V and $SrTiO_3$ capacitors. The capacitors with a high relative dielectric constant of 180 were employed. Under single 2.2 V operation, the developed MMIC delivered an output power of 22.6 dBm (182 mW) and a power-added efficiency of 33.2 % with an associated gain of 22.7 dB at 2.48 GHz.

Introduction

A small-sized MMIC power amplifier, which can be operated at a single low-voltage DC supply, is required for wireless local area network (WLAN) systems. Although several MMIC power amplifiers for WLAN have been reported[1,2], single low voltage operation of less than 3 V with more than 100 mW output power has not been reported yet. In addition, miniaturization of an MMIC power amplifier chip has been hampered due to the large area of its passive elements. In this paper, a single 2.2 V operation has been accomplished for a two-stage MMIC power amplifier with 0.76× 0.96 mm² area.

Design and fabrication

Figure 1 shows a schematic cross section of the developed MMIC. The one-chip MMIC consists of a 2 stage n-AlGaAs/InGaAs/n-AlGaAs heterojunction FET (HJFET) amplifier with input and output matching circuits as well as gate bias circuits utilizing $SrTiO_3$ (STO) capacitors.

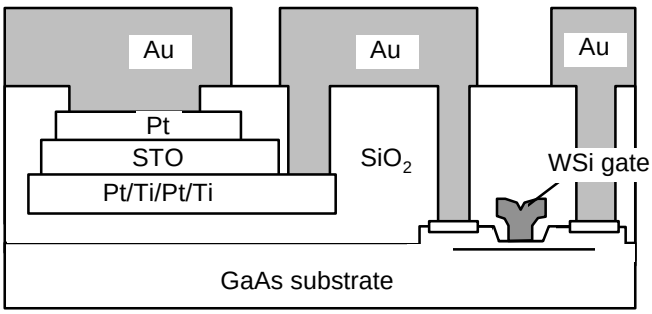

Fig.1 Cross section of the developed MMIC

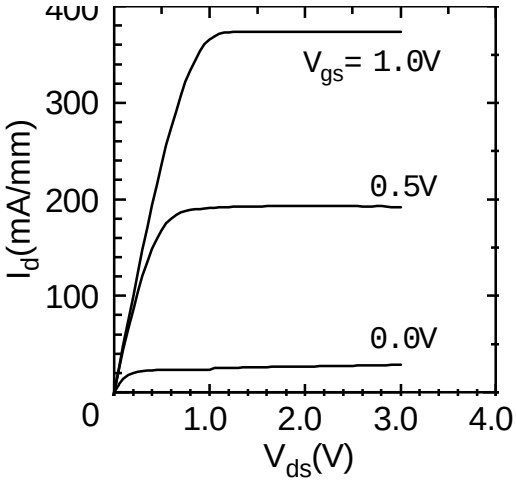

Fig.2 Drain I-V characteristics of the HJFET

Figure 2 shows the drain current (I_d) vs. drain-to-source voltage (V_{ds}) characteristics for the HJFET employed. The HJFET exhibited a maximum drain current of 370 mA/mm at a gate-to-source voltage (V_{gs}) of 1.5 V. The gate-to-drain breakdown voltage defined at a gate current of -1mA/mm was 20 V. Figure 3 shows the transconductance (gm) and I_d as a function of V_{gs} of the HJFET. The threshold voltage (V_T) was -0.24 V. This shallow V_T is essential for single voltage operation[3]. A double recess structure was fabricated by dry etching with an electron cyclotron resonance source, and the resulting standard deviation of V_T was as small as 20 mV on a 3 inch wafer. The capacitor consists of a Pt/Ti/Pt/Ti base metal electrode, a 200 nm-thick STO film and a Pt top electrode. This base electrode has high tolerance against ion-milling for capacitor fabrication, resulting in low series resistance[4]. The STO film was deposited at a substrate temperature of 450 °C before the HJFET fabrication. The STO film exhibited relative dielectric constant (ε_r) of 180. The capacitor fabricated in this process was reported to exhibit a high ε_r up to 20 GHz[4]. Figure 4 shows the I-V characteristics of the STO capacitor whose electrode area is 50 × 50 μm^2. The breakdown voltage defined at a 10 mA/cm^2 leakage current was more than 50 V. A 5.3 μm-thick Au layer was plated on the electrodes of capacitors and inductors to reduce DC and

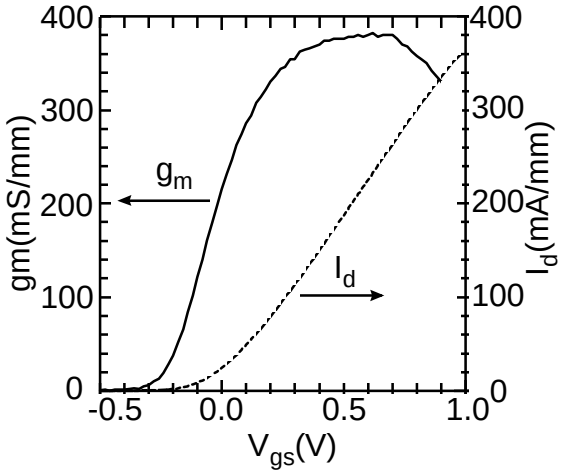

Fig.3 gm and I_d vs. V_{gs} of the HJFET

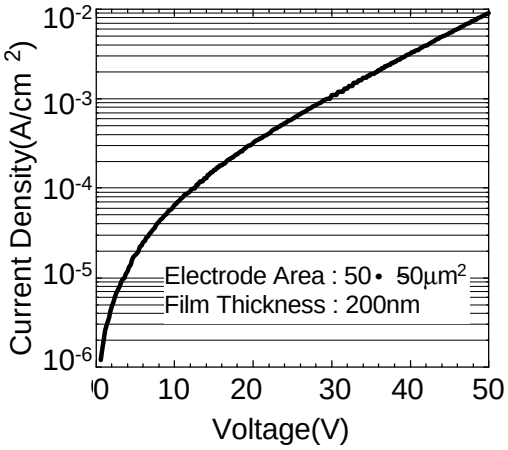

Fig.4 I-V Characteristics of the STO capacitor

RF losses.

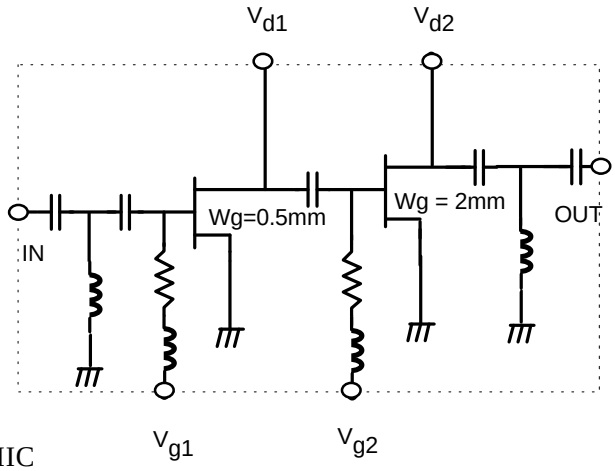

Figure 5 shows a circuit diagram of the MMIC power amplifier. The gate widths for the first stage and the second stage HJFETs are 0.5 and 2.0 mm, respectively. The input matching circuit is designed for maximum gain, and the output matching circuit is designed for maximum output power. For the output matching circuit, a series C and shunt L matching circuit with a coupling capacitor (CLC circuit) is employed. Since small area capacitors are available employing high ε_r STO films, the output matching circuit area is 0.05 mm^2, whereas the area of a conventional series L and

Fig.5 Circuit diagram of the MMIC power amplifier

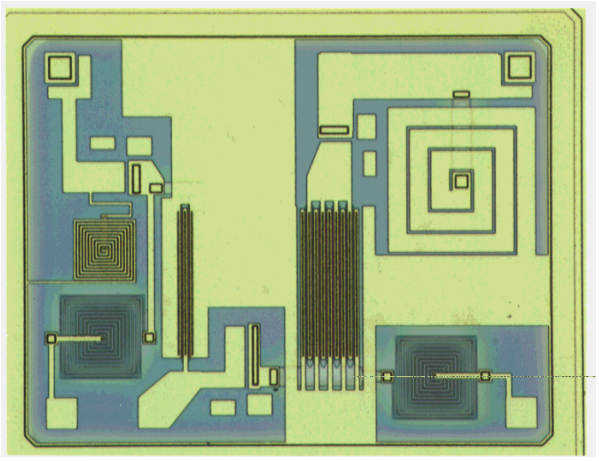

Fig.6 Chip photograph of the MMIC power amplifier

shunt C matching circuit with a coupling capacitor (LCCcircuit) employing SiN_x capacitors was 0.18 mm^2. Thus the CLC circuit with STO capacitors reduces 70 % of output matching circuit area as compared to the conventional one. Figure 6 shows the chip photograph for the MMIC power amplifier. The chip size is 0.796 × 0.796 mm^2.

MMIC Power Performance

The MMIC amplifier was operated at a drain supply voltage (V_{d1}, V_{d2}) of 2.2 V with gate bias voltages for the first FET (V_{gs1}) of +0.3 and the second FET (V_{gs2}) of +0.1 V. Bias voltages can be supplied by two Ni-MH battery cells without using a negative bias circuit. Figure 7 shows a 2.48 GHz power performance of the MMIC amplifier. The MMIC exhibited an output

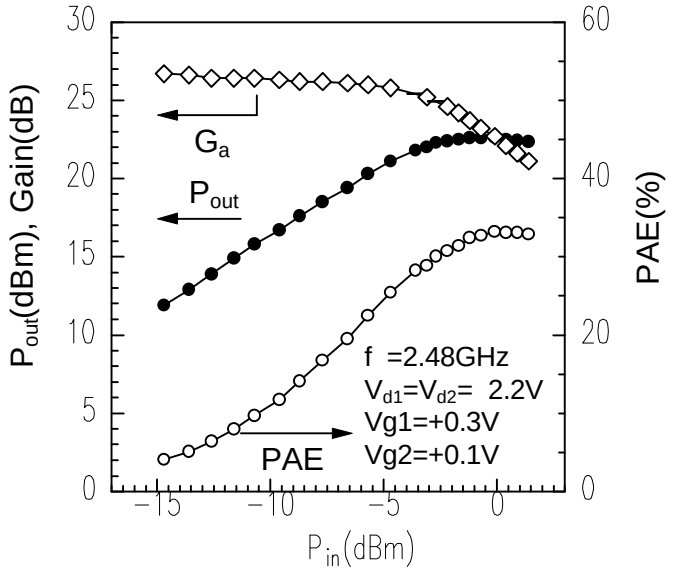

Fig.7 P_{out}, PAE and G_a vs. P_{in} for the MMIC amplifier

power of 22.6 dBm (182 mW) and a power-added efficiency of 33.2 % with an associated gain of 22.7 dB. To our knowledge, this is the first report of a GaAs MMIC power amplifier operated at single low voltage less than 3 V for WLAN applications.

Summary

A single 2.2 V operation two-stage MMIC power amplifier with 0.76×0.96 mm^2 area has been developed. n-AlGaAs/InGaAs/n-AlGaAs FETs with shallow V_T of

-0.24 V and $SrTiO_3$ capacitors with a high ε_r of 180 were employed. Operated at single 2.2 V, the MMIC delivered

22.6 dBm (182 mW) output power and 33.2 % power added efficiency with 22.7 dB associated gain at 2.48 GHz. The developed MMIC amplifier is promising for miniaturized WLAN applications.

Acknowledgments

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